REMARKS

The Office Action dated April 4, 2007 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claim 1 has been amended to more particularly point out an distinctly claim the subject matter of the invention. Claim 12 has been amended to correct a minor typographical error therein. No new matter has been added.

Claims 1-10, 12-26, and 28-33 are currently pending in the application. Claims 12-26 and 28-33 have been allowed. Applicants wish to thank the Examiner for the allowance of these claims. Claims 1-10, however, are respectfully submitted for consideration.

Claims 1-10 were rejected under 35 U.S.C. §102(e) as being anticipated by Headrick (U.S. Patent No. 5,724,358). The rejection is respectfully traversed for at least the following reasons.

Claim 1, upon which claims 2-10 are dependent, recites a network switch comprising at least one data port interface, a first memory, a second memory, and a memory management unit. The memory management unit is in connection with the at least one data port interface, the first memory, and the second memory. The memory management unit receives data from the at least one data port interface, determines if the data is to be stored in one of the first memory or the second memory, stores the data in one of the first memory or the second memory as a linked list, retrieves the data from one

of the first memory or the second memory, and forwards the data for egress. The memory management unit further includes a communication channel and a data input section in connection with the communication channel. The data input section further includes at least one cell accumulation buffer and a slot assembly unit, the slot assembly unit is configured to receive cells from the at least one cell accumulation buffer and package the received cells into cell slots to be stored in the second memory.

As will be discussed below, Headrick fails to disclose or suggest all of the elements of the claims, and therefore fails to provide the features discussed above.

Headrick discloses a high speed packet-switched digital switch that has a switch with a shared memory architecture. The switch may have a memory controller including an output queue for each output port. Each output queue includes a plurality of priority level sub-queues for routing data packets having different priority levels. The memory controller routes and buffers data packets on a per port, per priority level basis. The data packet has a header portion identifying one output port destination and a level of priority of the data within the packet. A buffer, shared by the output ports, stores the data packet in a selected buffer location based on the output port destination and priority level of the data packet. The data packets are output to the output ports in priority order.

Applicants respectfully submit that Headrick fails to disclose or suggest all of the elements of claim 1. For example, Headrick does not disclose or suggest that "when the data is stored in the second memory, global storage of data is initialized and continued until a last slot is stored," as recited in claim 1.

Headrick only discloses a first memory manager which process cells for ports 0-7 and a second memory manager which processes cells for ports 8-15. The number of memory managers may be increased or decreased depending upon the number of input ports for the particular switch (Headrick, Column 7, lines 1-6). In addition, Headrick discloses that each memory manager has a dedicated pointer memory unit associated with it (Headrick, Column 7, lines 25-27 and Fig. 7). Thus, according to Headrick, incoming ATM cells for ports 0-7 are processed by a first memory manager, while incoming cells for ports 8-15 are processed by the second memory manager. Each memory manager has a pointer memory unit associated with it and the cell will be stored in that memory unit.

However, Headrick makes no mention of initializing and continuing storage of global data when the data is to be stored in the second memory. Accordingly, Applicants respectfully submit that Headrick fails to disclose or suggest that "when the data is stored in the second memory, global storage of data is initialized and continued until a last slot is stored," as recited in claim 1. For at least the reasons discussed above, therefore, Applicants respectfully request that the rejection of claim 1 be withdrawn.

Claims 2-10 are dependent upon claim 1. Therefore, Applicants respectfully submit that claims 2-10 should be allowed for at least their dependence upon claim 1, and for the specific limitations recited therein.

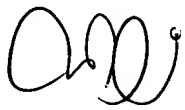
Applicants respectfully submit that Headrick fails to disclose or suggest all of the elements of the claimed invention. These distinctions are more than sufficient to render

the claimed invention unanticipated and unobvious. It is therefore respectfully requested that all of claims 1-10, 12-26 and 28-33 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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